REMARKS

Claims 1, 2, 4, 7-9, 11-15, 17, 18, and 22-24 are all the claims pending in the application. Claims 1, 7, and 15 are independent. This Amendment amends claims 1, 7, 12, 15, 18, 22, and 23, adds claim 24, cancels claims 5, 6, 10, 19-21 (without prejudice), and addresses each point of rejection raised by the Examiner. Favorable reconsideration is respectfully requested.

As an editorial matter, applicants have amended claim 22.

Claims 1-2, 4-15, and 17-23 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,420,992 to Killian *et al.* ("Killian").

Killian does not have flags or signals similar to the address format control flag/signal of the claimed invention. Address extension in Killian is a static decision (hardwired), not dynamic (flag controlled). For example, referring to the passage at column 3, line 67 to column 4, line 10 of Killian, Killian either does or does not extend an address. The extension can be either sign extension or zero extension depending upon the circuitry -- the type of circuitry is a design choice based upon whether timing constraints militate against sign-extension.

For example, consider the function of multiplexer 172 in FIG. 5D of Killian. Multiplexer 172 is interposed in the address path and zero extends the address depending upon a setting of a "32-bit user mode" signal. The 32-bit user mode signal indicates whether the address is 64 or 32 bits. While such a control signal is functionally similar to applicants' address space control flag (claim 9, 18), it bears no resemblance to a format control signal which specifies whether to zero extend or sign extend.

In this regards, applicants disagree with the Examiner's assertion in paragraph 13 of the Action that "This signal, when set, would indicate that addresses should be zero-extended and when cleared would indicate that addresses should be sign-extended." When Killian's 32-bit user mode signal is set, it does instruct multiplexer 172 to zero-extend a 32-bit mode address. However, when the 32-bit user control is clear, it indicates 64-bit mode, such that multiplexer 172 does not extend the address. Whether or not the 32-bit user control signal is set, a 16-bit offset is sign-extended to 64-bits, prior to the offset being added to a base address. However, the sign-extension of the 16-bit offset is not sign-extension of a *truncated* generated address reference, as described in the claims.

Further, the Examiner states that the claims do not exclude timing constraints as being a factor in choosing zero or sign extension. The sentence at column 4, lines 2-4 of Killian describes a fixed element of processor-design -- not a process step performed by the device.

Including the address format control flag facilitates support for multiple operating systems in the same processor by indicating whether an operating system uses a signed or an unsigned address space. In comparison, Killian does not appear to have recognized a need for flag-controlled extension.

Thus, referring to claim 1 (pre-amendment) as an example, Killian does not disclose the "means for extending" since Killian's address extension circuitry is only capable of sign extension *or* zero extension, but does not have settings for sign extension and zero extension, as described in the claim.

Reconsideration on the merits is requested.

Although it is applicants' position that the existing independent claims are patentably distinct from Killian for at least the reasons above, applicants have amended the independent claims to further describe address extension. Claim 1 is amended to incorporate the subject matter of claims 5 and 6; claim 7 is amended to incorporate the subject matter of claim 10; and claim 15 is amended to incorporate the subject matter of claims 19-21. As amended, each of the independent claims describes determining whether the address space is signed or unsigned based on a setting of an address format control signal/flag, and either zero-extending or sign-extending the address based on this determination. Consideration of the amended claims is also requested.

Additionally, referring to claims 12 and 23, Killian does not disclose the address fault control flag. According to an embodiment of the present invention, whether or not the processor checks for faults depends upon a setting of the address fault control flag. *See, e.g.,* pages 6 and 7 of the disclosure. By including an address fault control flag, fault generation can be selectively turned on by a debugger to help detect problems in porting an application to a larger-bit environment. Killian discloses a way to detect errors but discloses no flag to dynamically ignore or accept them.

Applicants have amended claims 12 and 23 to elaborate upon the function of the address fault control flag. Claim 24 is added to depend from claim 4 and add similar subject matter. Consideration of amended claims 12 and 23 and new claim 24 is requested.

Applicants authorize the Commissioner to charge any fees determined to be due with the exception of the issue fee and to credit any overpayment to Deposit Account No. 11-0600.

The Examiner is invited to contact the undersigned at (202) 220-4209 to discuss any matter concerning this application.

Respectfully submitted,
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